A1

the inductor includes a first terminal coupled to the third terminal of the transistor and a second terminal coupled to receive the RF input signal.

3. An RF mixer according to claim 2 further including a current source coupled to the second terminal of the inductor.

9. (Amended once) An RF mixer comprising:

SUBC1

a mixer core having a first input terminal for receiving a first current signal and a second input terminal for receiving a second current signal;

a first subcell coupled to the first input terminal of the mixer core to provide the first current signal to the mixer core responsive to an RF input signal, the first subcell having a first transistor and a first inductor coupled to the first transistor to extend the dynamic range

A2

of the mixer; and

a second subcell coupled to the second input terminal of the mixer core to provide a second current signal to the mixer core responsive to an RF input signal, the second subcell having a second transistor and a second inductor coupled to the first transistor to extend the dynamic range of the mixer;

wherein:

the first transistor includes a first terminal coupled to the first input terminal, a second terminal coupled to receive a reference signal, and a third terminal; and

the inductor includes a first terminal coupled to the third terminal of the transistor and a second terminal coupled to receive the RF input signal.

10. An RF mixer according to claim 9 wherein:

the second transistor is diode connected; and

the second inductor is arranged to degenerate the transconductance of the second transistor.

13. (Amended once) A current mirror comprising:

SUBC1

A3

a first transistor having a first terminal and a second terminal coupled together to cause the first transistor to operate as a diode, and a third terminal coupled to a common node;

a first inductor coupled between an input terminal and the first terminal of the first transistor to reduce the noise of the current mirror;

A3

a second transistor having a first terminal for transmitting an output signal, a second terminal coupled to the input terminal, and a third terminal; and

a second inductor coupled between the third terminal of the second transistor and a common node to reduce the noise of the current mirror.

Please add the following new claims:

SUBC7

15. (New) An amplifier cell comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal.

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16. (New) An amplifier cell according to claim 15 wherein the first class AB input stage comprises:

a first transistor having a first terminal coupled to the first output terminal, a second terminal coupled to recieve a bias signal, and a third terminal coupled to receive the first input signal; and

a first current mirror coupled between the first input terminal and the second output terminal.

17. (New) An amplifier cell according to claim 16 wherein the first class AB input stage further comprises a first inductor coupled between the input terminal and the third terminal of the first transistor.

18. (New) An amplifier cell according to claim 17 wherein the first class AB input stage further comprises a second inductor coupled between the input terminal and the current mirror.

19. (New) An amplifier cell according to claim 16 wherein the current mirror comprises at least one inductor arranged to reduce the noise of the current mirror.

20. (New) An amplifier cell according to claim 16 wherein the second class AB input stage comprises:

a second transistor having a first terminal coupled to the second output terminal, a second terminal coupled to recieve a bias signal, and a third terminal coupled to receive the second input signal; and

a second current mirror coupled between the second input terminal and the first output terminal.

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21. (New) An amplifier cell according to claim 20 wherein the second class AB input stage comprises at least one inductor arranged to reduce the noise of the input stage.

22. (New) An amplifier cell according to claim 15 wherein each of the class AB input stages comprises:

a common base transistor coupled between a first one of the input terminals;

an inductor coupled between the common base transistor and a first one of the ouput terminals; and

an inductively degenerated current mirror coupled between the first one of the input terminals and the other output terminal.

23. (New) An RF input section for a mixer, the RF input section comprising:

a first output terminal for coupling a first current to a mixer core;

a second output terminal for coupling a second current to the mixer core;

a first transistor having a first terminal coupled to the first output terminal, a second terminal coupled to receive a bias signal, and a third terminal coupled to a first RF input terminal for receiving a first RF input signal;

a first diode coupled between the first RF input terminal and a common node;

a second transistor having a first terminal coupled to the second output terminal, a second terminal coupled to form a current mirror with the first diode, and a third terminal coupled to the common node;

a third transistor having a first terminal coupled to the second output terminal, a second terminal coupled to receive the bias signal, and a third terminal coupled to a second RF input terminal for receiving a second RF input signal;

a second diode coupled between the second RF input terminal and the common node; and

a fourth transistor having a first terminal coupled to the first output terminal, a second terminal coupled to form a current mirror with the second diode, and a third terminal coupled to the common node.

24. (New) An RF input section according to claim 23 further including:

a first inductor coupled between the third terminal of the first transistor and the first RF input terminal;

a second inductor coupled in series with the first diode;

a third inductor coupled between the third terminal of the third transistor and the second RF input terminal; and

a fourth inductor coupled in series with the second diode.

25. (New) An RF input section according to claim 24 further including:

a fifth inductor coupled between the third terminal of the second transistor and the common node; and

a sixth inductor coupled between the third terminal of the fourth transistor and the common node.

26. (New) An RF input section according to claim 23 further including:

a sense node resistively coupled to the first and second diodes;

a delta-Vbe cell referenced to the common node and having first and second load input terminals for loading the cell, and a sense terminal coupled to the sense node;

a fifth transistor having a first terminal coupled to the common node, a second terminal coupled to the second load input terminal, and a third terminal coupled to the second terminal of the first transistor to provide the bias signal.